

Hdl Chip Design Smith

Bruce Wile,John Goss,Wolfgang Roesner

HDL Chip Design Douglas J. Smith,1996

Real Chip Design and Verification Using Verilog and VHDL Ben Cohen,2002 This book concentrates on common classes of hardware architectures and design problems, and focuses on the process of transitioning design requirements into synthesizable HDL code. Using his extensive, wide-ranging experience in computer architecture and hardware design, as well as in his training and consulting work, Ben provides numerous examples of real-life designs illustrated with VHDL and Verilog code. This code is shown in a way that makes it easy for the reader to gain a greater understanding of the languages and how they compare. All code presented in the book is included on the companion CD, along with other information, such as application notes.

Verilog Hdl Synthesis, a Practical Primer J. Bhasker,2018-05-21 With this book, you can: - Start writing synthesizable Verilog models quickly. - See what constructs are supported for synthesis and how these map to hardware so that you can get the desired logic. - Learn techniques to help avoid having functional mismatches. - Immediately start using many of the models for commonly used hardware elements described for your own use or modify these for your own application.

Verilog Styles for Synthesis of Digital Systems David Richard Smith,Paul D. Franzon,2000 This book is designed specifically to make the cutting-edge techniques of digital hardware design more accessible to those just entering the field. The text uses a simpler language (Verilog) and standardizes the methodology to the point where even novices can get medium complex designs through to gate-level simulation in a short period of time. Requires a working knowledge of computer organization, Unix, and X windows. Some knowledge of a programming language such as C or Java is desirable, but not necessary. Features a large number of worked examples and problems--from 100 to 100k gate equivalents--all synthesized and successfully verified by simulation at gate level using the VCS compiled simulator, the FPGA Compiler and Behavioral Compiler available from Synopsys, and the FPGA tool suites from Altera and Xilinx. Basic Language Constructs. Structural and Behavioral Specification. Simulation. Procedural Specification. Design Approaches for Single Modules. Validation of Single Modules. Finite State Machine Styles. Control-Point Writing Style. Managing Complexity--Large Designs. Improving Timing, Area, and Power. Design Compiler. Synthesis to Standard Cells. Synthesis to FPGA. Gate Level Simulation and Testing. Alternative Writing Styles. Mixed Technology Design. For anyone wanting an accessible, accelerated

introduction to the cutting-edge tools for Digital Hardware Design.

Digital System Test and Testable Design Zainalabedin Navabi, 2010-12-10 This book is about digital system testing and testable design. The concepts of testing and testability are treated together with digital design practices and methodologies. The book uses Verilog models and testbenches for implementing and explaining fault simulation and test generation algorithms. Extensive use of Verilog and Verilog PLI for test applications is what distinguishes this book from other test and testability books. Verilog eliminates ambiguities in test algorithms and BIST and DFT hardware architectures, and it clearly describes the architecture of the testability hardware and its test sessions. Describing many of the on-chip decompression algorithms in Verilog helps to evaluate these algorithms in terms of hardware overhead and timing, and thus feasibility of using them for System-on-Chip designs. Extensive use of testbenches and testbench development techniques is another unique feature of this book. Using PLI in developing testbenches and virtual testers provides a powerful programming tool, interfaced with hardware described in Verilog. This mixed hardware/software environment facilitates description of complex test programs and test strategies.

Hardware Description Language Demystified Dr. Cherry Sarma Bhargava, Dr. Rajkumar, 2020-09-03 Get familiar and work with the basic and advanced Modeling types in Verilog HDL Key Features a- Learn about the step-wise process to use Verilog design tools such as Xilinx, Vivado, Cadence NC-SIM a- Explore the various types of HDL and its need a- Learn Verilog HDL modeling types using examples a- Learn advanced concept such as UDP, Switch level modeling a- Learn about FPGA based prototyping of the digital system Description Hardware Description Language (HDL) allows analysis and simulation of digital logic and circuits. The HDL is an integral part of the EDA (electronic design automation) tool for PLDs, microprocessors, and ASICs. So, HDL is used to describe a Digital System. The combinational and sequential logic circuits can be described easily using HDL. Verilog HDL, standardized as IEEE 1364, is a hardware description language used to model electronic systems. This book is a comprehensive guide about the digital system and its design using various VLSI design tools as well as Verilog HDL. The step-wise procedure to use various VLSI tools such as Xilinx, Vivado, Cadence NC-SIM, is covered in this book. It also explains the advanced concept such as User Define Primitives (UDP), switch level modeling, reconfigurable computing, etc. Finally, this book ends with FPGA based prototyping of the digital system. By the end of this book, you will understand everything related to digital system design. What will you learn a- Implement Adder, Subtractor, Adder-Cum-Subtractor using Verilog HDL a- Explore the various Modeling styles in Verilog HDL a- Implement Switch level modeling using Verilog HDL a- Get familiar with advanced modeling techniques in Verilog HDL a- Get to know more about FPGA based prototyping using Verilog HDL Who this book is for Anyone interested in Electronics and VLSI design and want to learn Digital System Design with Verilog HDL will find this book useful. IC developers can also use this book as a quick reference for Verilog HDL fundamentals & features. Table of Contents 1. An Introduction to VLSI Design

Tools 2. Need of Hardware Description Language (HDL) 3. Logic Gate Implementation in Verilog HDL 4. Adder-Subtractor Implementation Using Verilog HDL 5. Multiplexer/Demultiplexer Implementation in Verilog HDL 6. Encoder/Decoder Implementation Using Verilog HDL 7. Magnitude Comparator Implementation Using Verilog HDL 8. Flip-Flop Implementation Using Verilog HDL 9. Shift Registers Implementation Using Verilog HDL 10. Counter Implementation Using Verilog HDL 11. Shift Register Counter Implementation Using Verilog HDL 12. Advanced Modeling Techniques 13. Switch Level Modeling 14. FPGA Prototyping in Verilog HDL About the Author Dr. Cherry Bhargava is working as an associate professor and head, VLSI domain, School of Electrical and Electronics Engineering at Lovely Professional University, Punjab, India. She has more than 14 years of teaching and research experience. She is Ph.D. (ECE), IKGPTU, M.Tech (VLSI Design & CAD) Thapar University and B.Tech (Electronics and Instrumentation) from Kurukshetra University. She is GATE qualified with All India Rank 428. She has authored about 50 technical research papers in SCI, Scopus indexed quality journals, and national/international conferences. She has eleven books related to reliability, artificial intelligence, and digital electronics to her credit. She has registered five copyrights and filed twenty-two patents. Your LinkedIn Profile <https://in.linkedin.com/in/dr-cherry-bhargava-7315619> Dr. Rajkumar Sarma received his B.E. in Electronics and Communications Engineering from Vinayaka Mission's University, Salem, India & M.Tech degree from Lovely Professional University, Phagwara, Punjab and currently pursuing Ph.D. from Lovely Professional University, Phagwara, Punjab. Your LinkedIn Profile www.linkedin.com/in/rajkumar-sarma-213657126

Rapid Prototyping of Digital Systems James O. Hamblen, Michael D. Furman, 2007-05-08 Rapid Prototyping of Digital Systems, Second Edition provides an exciting and challenging laboratory component for an undergraduate digital logic design class. The more advanced topics and exercises are also appropriate for consideration at schools that have an upper level course in digital logic or programmable logic. Design engineers working in industry will also want to consider this book for a rapid introduction to FPLD technology and logic synthesis using commercial CAD tools, especially if they have not had previous experience with the new and rapidly evolving technology. Two tutorials on the Altera CAD tool environment, an overview of programmable logic, and a design library with several easy-to-use input and output functions were developed for this book to help the reader get started quickly. Early design examples use schematic capture and library components. VHDL is used for more complex designs after a short introduction to VHDL-based synthesis. A coupon is included with the text for purchase of the new UP 1X board. The additional logic and memory in the UP 1X's FLEX 10K70 is useful on larger design projects such as computers and video games. The second edition includes an update chapter on programmable logic, new robot sensors and projects, optional Verilog examples, and a meta assembler which can be used to develop assemble language programs for the computer designs in Chapters 8 and 13.

High-level Synthesis Michael Fingeroff, 2010 Are you an RTL or system designer that is currently using, moving, or

planning to move to an HLS design environment? Finally, a comprehensive guide for designing hardware using C++ is here. Michael Fingeroff's High-Level Synthesis Blue Book presents the most effective C++ synthesis coding style for achieving high quality RTL. Master a totally new design methodology for coding increasingly complex designs! This book provides a step-by-step approach to using C++ as a hardware design language, including an introduction to the basics of HLS using concepts familiar to RTL designers. Each chapter provides easy-to-understand C++ examples, along with hardware and timing diagrams where appropriate. The book progresses from simple concepts such as sequential logic design to more complicated topics such as memory architecture and hierarchical sub-system design. Later chapters bring together many of the earlier HLS design concepts through their application in simplified design examples. These examples illustrate the fundamental principles behind C++ hardware design, which will translate to much larger designs. Although this book focuses primarily on C and C++ to present the basics of C++ synthesis, all of the concepts are equally applicable to SystemC when describing the core algorithmic part of a design. On completion of this book, readers should be well on their way to becoming experts in high-level synthesis.

Design Through Verilog HDL T. R. Padmanabhan, B. Bala Tripura Sundari, 2003-11-05 A comprehensive resource on Verilog HDL for beginners and experts Large and complicated digital circuits can be incorporated into hardware by using Verilog, a hardware description language (HDL). A designer aspiring to master this versatile language must first become familiar with its constructs, practice their use in real applications, and apply them in combinations in order to be successful. Design Through Verilog HDL affords novices the opportunity to perform all of these tasks, while also offering seasoned professionals a comprehensive resource on this dynamic tool. Describing a design using Verilog is only half the story: writing test-benches, testing a design for all its desired functions, and how identifying and removing the faults remain significant challenges. Design Through Verilog HDL addresses each of these issues concisely and effectively. The authors discuss constructs through illustrative examples that are tested with popular simulation packages, ensuring the subject matter remains practically relevant. Other important topics covered include: Primitives Gate and Net delays Buffers CMOS switches State machine design Further, the authors focus on illuminating the differences between gate level, data flow, and behavioral styles of Verilog, a critical distinction for designers. The book's final chapters deal with advanced topics such as timescales, parameters and related constructs, queues, and switch level design. Each chapter concludes with exercises that both ensure readers have mastered the present material and stimulate readers to explore avenues of their own choosing. Written and assembled in a paced, logical manner, Design Through Verilog HDL provides professionals, graduate students, and advanced undergraduates with a one-of-a-kind resource.

The Design Warrior's Guide to FPGAs Clive Maxfield, 2004-06-16 Field Programmable Gate Arrays (FPGAs) are devices that provide a fast, low-cost way for embedded system designers to customize products and deliver new versions with

upgraded features, because they can handle very complicated functions, and be reconfigured an infinite number of times. In addition to introducing the various architectural features available in the latest generation of FPGAs, The Design Warrior's Guide to FPGAs also covers different design tools and flows. This book covers information ranging from schematic-driven entry, through traditional HDL/RTL-based simulation and logic synthesis, all the way up to the current state-of-the-art in pure C/C++ design capture and synthesis technology. Also discussed are specialist areas such as mixed hardware/software and DSP-based design flows, along with innovative new devices such as field programmable node arrays (FPNAs). Clive Max Maxfield is a bestselling author and engineer with a large following in the electronic design automation (EDA) and embedded systems industry. In this comprehensive book, he covers all the issues of interest to designers working with, or contemplating a move to, FPGAs in their product designs. While other books cover fragments of FPGA technology or applications this is the first to focus exclusively and comprehensively on FPGA use for embedded systems. First book to focus exclusively and comprehensively on FPGA use in embedded designs World-renowned best-selling author Will help engineers get familiar and succeed with this new technology by providing much-needed advice on choosing the right FPGA for any design project

Design Recipes for FPGAs: Using Verilog and VHDL Peter Wilson, 2011-02-24 Design Recipes for FPGAs: Using Verilog and VHDL provides a rich toolbox of design techniques and templates to solve practical, every-day problems using FPGAs. Using a modular structure, the book gives 'easy-to-find' design techniques and templates at all levels, together with functional code. Written in an informal and 'easy-to-grasp' style, it goes beyond the principles of FPGA s and hardware description languages to actually demonstrate how specific designs can be synthesized, simulated and downloaded onto an FPGA. This book's 'easy-to-find' structure begins with a design application to demonstrate the key building blocks of FPGA design and how to connect them, enabling the experienced FPGA designer to quickly select the right design for their application, while providing the less experienced a 'road map' to solving their specific design problem. The book also provides advanced techniques to create 'real world' designs that fit the device required and which are fast and reliable to implement. This text will appeal to FPGA designers of all levels of experience. It is also an ideal resource for embedded system development engineers, hardware and software engineers, and undergraduates and postgraduates studying an embedded system which focuses on FPGA design. A rich toolbox of practical FGPA design techniques at an engineer's finger tips Easy-to-find structure that allows the engineer to quickly locate the information to solve their FGPA design problem, and obtain the level of detail and understanding needed

Chip-level Modeling with VHDL James R. Armstrong, 1989

Writing Testbenches: Functional Verification of HDL Models Janick Bergeron, 2012-12-06 mental improvements during the same period. What is clearly needed in verification techniques and technology is the equivalent of a synthesis productivity breakthrough. In the second edition of Writing Testbenches, Bergeron raises the verification level of abstraction

by introducing coverage-driven constrained-random transaction-level self-checking testbenches all made possible through the introduction of hardware verification languages (HVLs), such as e from Verisity and OpenVera from Synopsys. The state-of-art methodologies described in Writing Test benches will contribute greatly to the much-needed equivalent of a synthesis breakthrough in verification productivity. I not only highly recommend this book, but also I think it should be required reading by anyone involved in design and verification of today's ASIC, SoCs and systems. Harry Foster Chief Architect Verplex Systems, Inc. xviii Writing Testbenches: Functional Verification of HDL Models PREFACE If you survey hardware design groups, you will learn that between 60% and 80% of their effort is now dedicated to verification.

System-on-Chip Methodologies & Design Languages Peter J. Ashenden, Jean Mermet, Ralf Seepold, 2013-03-14 System-on-Chip Methodologies & Design Languages brings together a selection of the best papers from three international electronic design language conferences in 2000. The conferences are the Hardware Description Language Conference and Exhibition (HDLCon), held in the Silicon Valley area of USA; the Forum on Design Languages (FDL), held in Europe; and the Asia Pacific Chip Design Language (APChDL) Conference. The papers cover a range of topics, including design methods, specification and modeling languages, tool issues, formal verification, simulation and synthesis. The results presented in these papers will help researchers and practicing engineers keep abreast of developments in this rapidly evolving field.

Principles of Verifiable RTL Design Lionel Bening, Harry D. Foster, 2007-05-08 System designers, computer scientists and engineers have continuously invented and employed notations for modeling, specifying, simulating, documenting, communicating, teaching, verifying and controlling the designs of digital systems. Initially these systems were represented via electronic and fabrication details. Following C. E. Shannon's revelation of 1948, logic diagrams and Boolean equations were used to represent digital systems in a fashion that de-emphasized electronic and fabrication detail while revealing logical behavior. A small number of circuits were made available to remove the abstraction of these representations when it was desirable to do so. As system complexity grew, block diagrams, timing charts, sequence charts, and other graphic and symbolic notations were found to be useful in summarizing the gross features of a system and describing how it operated. In addition, it always seemed necessary or appropriate to augment these documents with lengthy verbal descriptions in a natural language. While each notation was, and still is, a perfectly valid means of expressing a design, lack of standardization, conciseness, and formal definitions interfered with communication and the understanding between groups of people using different notations. This problem was recognized early and formal languages began to evolve in the 1950s when I. S. Reed discovered that flip-flop input equations were equivalent to a register transfer equation, and that vector-like notation. Expanding these concepts Reed developed a notation that became known as a Register Transfer Language (RTL).

Comprehensive Functional Verification Bruce Wile, John Goss, Wolfgang Roesner, 2005-05-26 One of the biggest challenges in chip and system design is determining whether the hardware works correctly. That is the job of functional

verification engineers and they are the audience for this comprehensive text from three top industry professionals. As designs increase in complexity, so has the value of verification engineers within the hardware design team. In fact, the need for skilled verification engineers has grown dramatically--functional verification now consumes between 40 and 70% of a project's labor, and about half its cost. Currently there are very few books on verification for engineers, and none that cover the subject as comprehensively as this text. A key strength of this book is that it describes the entire verification cycle and details each stage. The organization of the book follows the cycle, demonstrating how functional verification engages all aspects of the overall design effort and how individual cycle stages relate to the larger design process. Throughout the text, the authors leverage their 35 plus years experience in functional verification, providing examples and case studies, and focusing on the skills, methods, and tools needed to complete each verification task. Comprehensive overview of the complete verification cycle Combines industry experience with a strong emphasis on functional verification fundamentals Includes real-world case studies

Digital Design with Verilog® HDL Elizer Sternheim, Rajvir Singh, Yatin Trivedi, 1990 Verilog HDL is the standard hardware description language for the design of digital systems and VLSI devices. This volume shows designers how to describe pieces of hardware functionally in Verilog using a top-down design approach, which is illustrated with a number of large design examples. The work is organized to present material in a progressive manner, beginning with an introduction to Verilog HDL and ending with a complete example of the modelling and testing of a large subsystem.

Digital Design Frank Vahid, 2006 Digital Design provides a modern approach to learning the increasingly important topic of digital systems design. The text's focus on register-transfer-level design and present-day applications not only leads to a better appreciation of computers and of today's ubiquitous digital devices, but also provides for a better understanding of careers involving digital design and embedded system design. The book's key features include: An emphasis on register-transfer-level (RTL) design, the level at which most digital design is practiced today, giving readers a modern perspective of the field's applicability. Yet, coverage stays bottom-up and concrete, starting from basic transistors and gates, and moving step-by-step up to more complex components. Extensive use of basic examples to teach and illustrate new concepts, and of application examples, such as pacemakers, ultrasound machines, automobiles, and cell phones, to demonstrate the immediate relevance of the concepts. Separation of basic design from optimization, allowing development of a solid understanding of basic design, before considering the more advanced topic of optimization. Flexible organization, enabling early or late coverage of optimization methods or of HDLs, and enabling choice of VHDL, Verilog, or SystemC HDLs. Career insights and advice from designers with varying levels of experience. A clear bottom-up description of field-programmable gate arrays (FPGAs). About the Author: Frank Vahid is a Professor of Computer Science & Engineering at the University of California, Riverside. He holds Electrical Engineering and Computer Science degrees; has worked/consulted for Hewlett

Packard, AMCC, NEC, Motorola, and medical equipment makers; holds 3 U.S. patents; has received several teaching awards; helped setup UCR's Computer Engineering program; has authored two previous textbooks; and has published over 120 papers on digital design topics (automation, architecture, and low-power).

Advanced HDL Synthesis and SOC Prototyping Vaibhav Taraate, 2018-12-15 This book describes RTL design using Verilog, synthesis and timing closure for System On Chip (SOC) design blocks. It covers the complex RTL design scenarios and challenges for SOC designs and provides practical information on performance improvements in SOC, as well as Application Specific Integrated Circuit (ASIC) designs. Prototyping using modern high density Field Programmable Gate Arrays (FPGAs) is discussed in this book with the practical examples and case studies. The book discusses SOC design, performance improvement techniques, testing and system level verification, while also describing the modern Intel FPGA/XILINX FPGA architectures and their use in SOC prototyping. Further, the book covers the Synopsys Design Compiler (DC) and Prime Time (PT) commands, and how they can be used to optimize complex ASIC/SOC designs. The contents of this book will be useful to students and professionals alike.

Digital Design of Signal Processing Systems Shoab Ahmed Khan, 2011-02-02 Digital Design of Signal Processing Systems discusses a spectrum of architectures and methods for effective implementation of algorithms in hardware (HW). Encompassing all facets of the subject this book includes conversion of algorithms from floating-point to fixed-point format, parallel architectures for basic computational blocks, Verilog Hardware Description Language (HDL), SystemVerilog and coding guidelines for synthesis. The book also covers system level design of Multi Processor System on Chip (MPSoC); a consideration of different design methodologies including Network on Chip (NoC) and Kahn Process Network (KPN) based connectivity among processing elements. A special emphasis is placed on implementing streaming applications like a digital communication system in HW. Several novel architectures for implementing commonly used algorithms in signal processing are also revealed. With a comprehensive coverage of topics the book provides an appropriate mix of examples to illustrate the design methodology. Key Features: A practical guide to designing efficient digital systems, covering the complete spectrum of digital design from a digital signal processing perspective Provides a full account of HW building blocks and their architectures, while also elaborating effective use of embedded computational resources such as multipliers, adders and memories in FPGAs Covers a system level architecture using NoC and KPN for streaming applications, giving examples of structuring MATLAB code and its easy mapping in HW for these applications Explains state machine based and Micro-Program architectures with comprehensive case studies for mapping complex applications The techniques and examples discussed in this book are used in the award winning products from the Center for Advanced Research in Engineering (CARE). Software Defined Radio, 10 Gigabit VoIP monitoring system and Digital Surveillance equipment has respectively won APICTA (Asia Pacific Information and Communication Alliance) awards in 2010 for their unique and effective designs.

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